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RODELA, EDUARDO A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,253	PRZADKA, ANDREAS	
	Examiner	Art Unit	
	EDUARDO A. RODELA	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/17/2008*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination received July 21, 2008.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 10-13, 15, 17, 18-22, 23, 25, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083).

Regarding Claim 1, Ahn shows in Figure 1, an electronic component comprising:

a multi-layer substrate [10] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [106,110], the at least one integrated impedance converter comprising at least one inductor [106] and at least one capacitor [110] integrated in the multi-layer substrate [10], the mutli-layer substrate [10] comprising first external contacts [portion of 112 where 150 makes contact thereto] on the underside [bottom surface of 10]; and

at least one chip component [120] comprising external contacts [portion of 142 contacting 150], the at least one chip component being disposed on the upper side of the multi-layer substrate [10], the at least one chip component [120] being electrically

connected [150] to the at least one integrated impedance converter [150 connect to both 106,110],

the second external contacts [portion of 112 where 150 makes contact thereto] being electrically connected to the first external contacts via an impedance conversion circuit [106, 108, 110] that is at least partially integrated into the multilayer substrate [shown], the impedance conversion circuit comprising an inductive component [106] that is electrically connected to the first external contacts [portion of 112 where 150 makes contact thereto, column 8, lines 1-19];

wherein the at least one chip component comprises RF communication elements [column 2: lines 7-22 and column 6: lines 12-30].

Ahn does not show wherein the at least one chip component comprises a bulk acoustic wave (BAW) resonator or a surface acoustic wave (SAW) resonator.

Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] comprises a surface acoustic wave (SAW) resonator [column 7, lines 19-34]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable surface acoustic wave device of Uchikoba for use in the invention of Ahn, in order to further provide components capable of converting acoustic waves into electrical signals which are necessary for RF communications.

Ahn in view of Uchikoba do not show wherein the inductive component that is electrically connected is specifically in series between the first external contacts and the second external contacts.

Utsumi shows in Figure 8, wherein the inductive component [19] that is electrically connected is specifically in series [shown] between the first external contacts [lower contact] and the second external contacts [upper contact].

Utsumi teaches the benefit of this orientation as for, "The provision of the inductors in the via hole and the through hole results in increase in high frequency impedance without increase in direct current resistance to the circuit whereby the high frequency noises are prevented from reaching the power source circuit layer.", as shown on column 8, lines 42-47.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have connected the second end of the inductor of the system of Ahn in view of Uchikoba as taught by Utsumi, for the purpose of preventing high frequency noises from propagating within the device.

Ahn/Uchikoba/Utsumi do not show the specifics wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5%.

Ahn discusses the intent of the particular circuit in the invention as for converting incoming signals for the particular quality the RF circuit requires by use of a passive component network, however, the actual impedance values are not given.

Cave shows a chip in a package orientation where a passive component network is used to convert incoming signals specifically, wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% ["impedance matching" occurs wherein a 50 Ohm input

impedance is converted to a 5 Ohm output impedance, therefore 50 Ohms fed into the impedance matching circuit is converted to 5 Ohms, column 2, lines 59-63]. It is noted that these impedance conversions are typical for chip packages.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have had an orientation wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% in the system of Ahn/Uchikoba/Utsumi as taught by Cave, as it is well known in the art to "impedance match" external signals to the internal circuit network, for providing optimal signals to allow the internal circuits to function properly.

Regarding Claim 2, Ahn/Uchikoba/Utsumi/Cave show the electronic component of claim 1. In addition, Ahn shows in Figure 1 wherein the external contacts [portion of 142 contacting 150] comprise surface mounted device contacts [flip chip orientation shown].

Regarding Claim 3, Ahn/Uchikoba/Utsumi/Cave show the electronic component of claim 1. In addition, Ahn shows in Figure 1 wherein the multi-layer substrate [10] comprises at least one passive circuit element of at least one active circuit element [108].

Regarding claim 10, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. In addition Ahn shows wherein the at least one discrete circuit element [108] disposed on the upper side of the multi-layer substrate [10], the at least on discrete circuit element comprising an active circuit element or a passive circuit element [column 6, lines 56-65].

Regarding claim 11, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 10. Uchikoba does disclose in Figures 9-11, wherein the at least one discrete circuit element [15] comprises at least one of the following: an antenna circuit, a diplexer, a low pass filter, and a band pass filter [column 1, lines 52-67].

Regarding claim 12, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 10. Ahn shows in Figure 1, an electronic component comprising:

a multi-layer substrate [10] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [106,110], the at least one integrated impedance converter comprising at least one inductor [106] and at least one capacitor [110] integrated in the multi-layer substrate [10], the mutli-layer substrate [10] comprising first external contacts [portion of 112 where 150 makes contact thereto] on the underside [bottom surface of 10]; and

at least one chip component [120] comprising external contacts [portion of 142 contacting 150], the at least one chip component being disposed on the upper side of the multi-layer substrate [10], the at least one chip component [120] being electrically connected [150] to the at least one integrated impedance converter [150 connect to both 106,110],

the second external contacts [portion of 112 where 150 makes contact thereto] being electrically connected to the first external contacts via an impedance conversion circuit [106, 108, 110] that is at least partially integrated into the multilayer substrate [shown], the impedance conversion circuit comprising an inductive component [106] that

is electrically connected to the first external contacts [portion of 112 where 150 makes contact thereto, column 8, lines 1-19];

wherein the at least one chip component comprises RF communication elements [column 2: lines 7-22 and column 6: lines 12-30].

Ahn does not show wherein the at least one chip component comprises a bulk acoustic wave (BAW) resonator or a surface acoustic wave (SAW) resonator, and wherein the at least one discrete circuit element comprises at least part of a diplexer, and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an antenna.

Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] comprises a surface acoustic wave (SAW) resonator [column 7, lines 19-34]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable surface acoustic wave device of Uchikoba for use in the invention of Ahn, in order to further provide components capable of converting acoustic waves into electrical signals which are necessary for RF communications.

Uchikoba discloses in Figures 9-11, wherein the at least one discrete circuit element [15] comprises at least part of a diplexer [column 1, lines 52-67], and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an antenna [column 1, lines 53-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use the at least one discrete circuit element comprises at least part of a diplexer, and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an

antenna as in the device of Uchikoba for use in the invention of Ahn, in order to frequency domain multiplexing, which not having the several frequencies interfere with each other.

Ahn in view of Uchikoba do not show wherein the inductive component that is electrically connected is specifically in series between the first external contacts and the second external contacts.

Utsumi shows in Figure 8, wherein the inductive component [19] that is electrically connected is specifically in series [shown] between the first external contacts [lower contact] and the second external contacts [upper contact].

Utsumi teaches the benefit of this orientation as for, "The provision of the inductors in the via hole and the through hole results in increase in high frequency impedance without increase in direct current resistance to the circuit whereby the high frequency noises are prevented from reaching the power source circuit layer.", as shown on column 8, lines 42-47.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have connected the second end of the inductor of the system of Ahn in view of Uchikoba as taught by Utsumi, for the purpose of preventing high frequency noises from propagating within the device.

Ahn/Uchikoba/Utsumi do not show the specifics wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5%.

Ahn discusses the intent of the particular circuit in the invention as for converting incoming signals for the particular quality the RF circuit requires by use of a passive component network, however, the actual impedance values are not given.

Cave shows a chip in a package orientation where a passive component network is used to convert incoming signals specifically, wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% ["impedance matching" occurs wherein a 50 Ohm input impedance is converted to a 5 Ohm output impedance, therefore 50 Ohms fed into the impedance matching circuit is converted to 5 Ohms, column 2, lines 59-63]. It is noted that these impedance conversions are typical for chip packages.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have had an orientation wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% in the system of Ahn/Uchikoba/Utsumi as taught by Cave, as it is well known in the art to "impedance match" external signals to the internal circuit network, for providing optimal signals to allow the internal circuits to function properly.

Regarding claim 13, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Uchikoba does disclose in Figures 9-11, a low pass filter, a band pass filter, a diplexer [column 1, lines 53-67].

Regarding claim 15, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Uchikoba does disclose in Figures 9-11, wherein the multi-layer substrate [1] comprises a plurality of adjustment circuits [LPF,DPX,BPF].

Regarding claim 17, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Ahn does disclose wherein the multi-layer substrate [10] comprises layers of silicon or silicon oxide [column 6, lines 31-45].

Regarding claim 18, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Ahn does show wherein the multi-layer substrate [10] comprises one or more layers of an organic material [122, epoxy].

Regarding claim 19, Ahn/Uchikoba/Utsumi/Cave discloses the electronic component of claim 1. Uchikoba does disclose in Figures 9-11, wherein the at least one chip [15] comprises at least one or more inputs and outputs [inherently any operational device would]; and wherein at least one input and/or at least one output of the at least one chip component conducts an asymmetrical signal [components in the LPF and BPF would handle signals with a spectrum of frequencies].

Regarding claim 20, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Uchikoba does disclose wherein the at least one chip component comprises at least one or more inputs and outputs [inherently any operational device would]; and wherein at least one input and/or at least one output of the at least one chip component conducts a symmetrical signal [Fig. 9: the receiving circuit would have a clock signal, which is symmetrical].

Regarding claim 21, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Uchikoba does show in Figure 3 of which schematic components are all situated on the ceramic substrate, wherein the at least one chip component [downward facing diode] comprises a connection to ground [schematic

ground], the connection to ground being made via an adjustment circuit [parallel resistor and capacitor both connected to ground] that is at least partially integrally integrated in the multi-layer substrate [all schematic components are on the surface of the ceramic capacitor]; and wherein the adjustment circuit comprises a capacitor [capacitor in parallel with resistor both connected to ground] and a conductor.

Regarding claim 22, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 10. In addition Ahn shows wherein the at least one chip component [120] and the at least one discrete circuit element [108] comprise surface mounted design elements [designed to operate at the surface of 10].

Regarding claim 23, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. In addition Ahn shows wherein the at least one chip component [120] comprises a housing [portion of 122 contacting surface of 120] comprising external contacts [138].

Regarding claim 25, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. In addition, Ahn shows wherein the at least one chip component [120] is connected to the multi-layer substrate [10] via flip-chip technology [shown].

Regarding claim 26, Ahn shows in Figure 1, a method of producing an electronic component comprised of a multi-layer substrate [10] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [106,110], the at least one integrated impedance converter comprising at least one inductor [106] and at least one capacitor [110] integrated in the multi-layer substrate [10], the multilayer substrate comprising first external contacts on the under side

[portion of 112 where 150 meets], and at least one chip component [120] comprising second external contacts [portions of 142 contacting 150 on upper side], the method comprising:

installing the at least one chip component [120] in a housing [portion of 122 contacting 120]; and

mounting the housing onto the upper side of the multilayer substrate [10] so as to electrically connect the at least one chip component [120] to the integrated impedance converter [106,110].

the second external contacts [portion of 112 where 150 makes contact thereto] being electrically connected to the first external contacts via an impedance conversion circuit [106, 108, 110] that is at least partially integrated into the multilayer substrate [shown], the impedance conversion circuit comprising an inductive component [106] that is electrically connected to the first external contacts [portion of 112 where 150 makes contact thereto, column 8, lines 1-19];

wherein the at least one chip component comprises RF communication elements [column 6, lines 25-30 and column 8, lines 35-40].

Ahn does not show wherein the at least one chip component comprises a bulk acoustic wave (BAW) resonator or a surface acoustic wave (SAW) resonator.

Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] comprises a surface acoustic wave (SAW) resonator [column 7, lines 19-34]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable surface acoustic wave device of Uchikoba for use in

the invention of Ahn, in order to further provide components capable of converting acoustic waves into electrical signals which are necessary for RF communications.

Ahn in view of Uchikoba do not show wherein the inductive component that is electrically connected is specifically in series between the first external contacts and the second external contacts.

Utsumi shows in Figure 8, wherein the inductive component [19] that is electrically connected is specifically in series [shown] between the first external contacts [lower contact] and the second external contacts [upper contact].

Utsumi teaches the benefit of this orientation as for, "The provision of the inductors in the via hole and the through hole results in increase in high frequency impedance without increase in direct current resistance to the circuit whereby the high frequency noises are prevented from reaching the power source circuit layer.", as shown on column 8, lines 42-47.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have connected the second end of the inductor of the system of Ahn in view of Uchikoba as taught by Utsumi, for the purpose of preventing high frequency noises from propagating within the device.

Ahn/Uchikoba/Utsumi do not show the specifics wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5%.

Ahn discusses the intent of the particular circuit in the invention as for converting incoming signals for the particular quality the RF circuit requires by use of a passive component network, however, the actual impedance values are not given.

Cave shows a chip in a package orientation where a passive component network is used to convert incoming signals specifically, wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% ["impedance matching" occurs wherein a 50 Ohm input impedance is converted to a 5 Ohm output impedance, therefore 50 Ohms fed into the impedance matching circuit is converted to 5 Ohms, column 2, lines 59-63]. It is noted that these impedance conversions are typical for chip packages.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have had an orientation wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% in the system of Ahn/Uchikoba/Utsumi as taught by Cave, as it is well known in the art to "impedance match" external signals to the internal circuit network, for providing optimal signals to allow the internal circuits to function properly.

Regarding claim 27, Ahn/Uchikoba/Utsumi/Cave in further view of Utsumi disclose the method of claim 26. In addition, Ahn shows comprising: mounting at least one discrete circuit element [108] on the upper side of the multi-layer substrate [10].

Regarding claim 28, Ahn/Uchikoba/Utsumi/Cave in further view of Utsumi disclose the method of claim 27. Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] and the at least one discrete circuit element [50] are

attached to the upper side of the multi-layer substrate [40] using a same attaching mechanism [surface mount connection].

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in further view of Chakravorty (US 6,970,362).

Regarding Claim 4, Ahn/Uchikoba/Utsumi/Cave show the electronic component of claim 1. Ahn/Uchikoba/Utsumi/Cave doe not specify wherein the at least one chip component comprises at least one filter circuit. Ahn does however discuss that, “the digital circuit elements 140 of the chips 120 form the required analog and digital circuitry for an analog / digital RF communication system.” It is well known in the art that RF communication systems require at least some filter circuits for basic operation. Chakravorty does disclose in Figure 2, a multilayer substrate [55] with a die [40], surface mounted on the upper surface, wherein the at least one chip component comprising at least one filter circuit [column 3, lines 60-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made that the chip component of Ahn/Uchikoba/Utsumi/Cave could have any sort of circuit therein such as a filter circuit of Chakravorty, in order to further provide components capable of converting radio signals into electrical signals and visa verse, which is a necessary functionality for a RF communications device.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in view of Li (US 6,713,860).

Regarding claim 7, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Ahn/Uchikoba/Utsumi/Cave does not disclose wherein the at least one chip component comprises a microwave ceramic filter. Li discloses in Figure 5, the use of a ceramic capacitor [506, column 13, lines 52-60] that is surface mounted on a multilayer substrate [502]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to (1) have a ceramic capacitor of Li in a microwave ceramic filter and (2) have a microwave ceramic filter on the substrate of the system of Ahn/Uchikoba/Utsumi/Cave, in order to provide components necessary for the operation of a microwave frequency ceramic filter.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in view of Asahi et al. (US 6,955,948).

Regarding claim 8 Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1, and that it contains inductors, capacitors, and resistors [column 13, lines 55-65]. Ahn/Uchikoba/Utsumi/Cave do not specifically disclose a LC chip filter. Asahi et al. discloses the at least one chip component comprises an inductive-capacitive (LC) chip

filter [column 9: lines 10-17]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a LC filter in a high frequency circuit used in receiving and transmitting circuits. The ordinary artisan would have been motivated to use the LC filter in the system of Ahn/Uchikoba/Utsumi/Cave as suggested by Asahi to provide the necessary filtering, modulation, and various other signal shaping functions necessary to the task.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in even further view of Figueroa et al. (US 6,388,207).

Regarding claim 9, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Ahn in view of Uchikoba in further view of Utsumi do not show a stripline filter. Figueroa et al. discloses the at least one chip component comprises a stripline filter [capacitor used as signal filter to deliver improved signal integrity through the substrate to the semiconductor chips, disclosed in column 3: lines 24-34, column 4: lines 1-10, and column 6: lines 24-34]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stripline filter of Figueroa in the substrate of the system of Ahn/Uchikoba/Utsumi/Cave, in order to improve the signal quality being fed through the substrate to the supported electronic component.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in further view of Liu et al. (US 6,060,954).

Regarding claim 14, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 13.

Ahn shows in Figure 1, an electronic component comprising:

a multi-layer substrate [10] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [106,110], the at least one integrated impedance converter comprising at least one inductor [106] and at least one capacitor [110] integrated in the multi-layer substrate [10], the mutli-layer substrate [10] comprising first external contacts [portion of 112 where 150 makes contact thereto] on the underside [bottom surface of 10]; and

at least one chip component [120] comprising external contacts [portion of 142 contacting 150], the at least one chip component being disposed on the upper side of the multi-layer substrate [10], the at least one chip component [120] being electrically connected [150] to the at least one integrated impedance converter [150 connect to both 106,110],

the second external contacts [portion of 112 where 150 makes contact thereto] being electrically connected to the first external contacts via an impedance conversion circuit [106, 108, 110] that is at least partially integrated into the multilayer substrate [shown], the impedance conversion circuit comprising an inductive component [106] that

is electrically connected to the first external contacts [portion of 112 where 150 makes contact thereto, column 8, lines 1-19];

wherein the at least one chip component comprises RF communication elements [column 2: lines 7-22 and column 6: lines 12-30].

Ahn does not show wherein the at least one chip component comprises a bulk acoustic wave (BAW) resonator or a surface acoustic wave (SAW) resonator.

Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] comprises a surface acoustic wave (SAW) resonator [column 7, lines 19-34]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable surface acoustic wave device of Uchikoba for use in the invention of Ahn, in order to further provide components capable of converting acoustic waves into electrical signals which are necessary for RF communications.

Ahn in view of Uchikoba do not show wherein the inductive component that is electrically connected is specifically in series between the first external contacts and the second external contacts.

Utsumi shows in Figure 8, wherein the inductive component [19] that is electrically connected is specifically in series [shown] between the first external contacts [lower contact] and the second external contacts [upper contact].

Utsumi teaches the benefit of this orientation as for, "The provision of the inductors in the via hole and the through hole results in increase in high frequency impedance without increase in direct current resistance to the circuit whereby the high

frequency noises are prevented from reaching the power source circuit layer.", as shown on column 8, lines 42-47.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have connected the second end of the inductor of the system of Ahn in view of Uchikoba as taught by Utsumi, for the purpose of preventing high frequency noises from propagating within the device.

Ahn/Uchikoba/Utsumi do not show the specifics wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5%.

Ahn discusses the intent of the particular circuit in the invention as for converting incoming signals for the particular quality the RF circuit requires by use of a passive component network, however, the actual impedance values are not given.

Cave shows a chip in a package orientation where a passive component network is used to convert incoming signals specifically, wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by at least 5% ["impedance matching" occurs wherein a 50 Ohm input impedance is converted to a 5 Ohm output impedance, therefore 50 Ohms fed into the impedance matching circuit is converted to 5 Ohms, column 2, lines 59-63]. It is noted that these impedance conversions are typical for chip packages.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have had an orientation wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip

component by at least 5% in the system of Ahn/Uchikoba/Utsumi as taught by Cave, as it is well known in the art to "impedance match" external signals to the internal circuit network, for providing optimal signals to allow the internal circuits to function properly.

Ahn/Uchikoba/Utsumi/Cave do not show wherein the at least part of an adjustment circuit integrated in the multi-layer substrate is formed as one or more strip conductors on the upper side of the multi-layer substrate. Liu et al. do disclose in Figure 2B and 2F, wherein the at least part of an adjustment circuit [column 2, lines 40-45] integrated in the multi-layer substrate is formed as one or more strip conductors [101] on the upper side of the multi-layer substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stripline conductor of Liu on the upper surface of the substrate of the system of Ahn/Uchikoba/Utsumi/Cave, in order to allow for the re-workability of the circuit and simplify the fabrication process with respect to the substrate, rather than burying the conductors, making vias, and bonding pads.

Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in view of Daniels et al. (US 6,642,811).

Regarding claim 16, Ahn/Uchikoba/Utsumi/Cave disclose the electronic component of claim 1. Ahn in view of Uchikoba in further view of Utsumi do not show wherein the multi-layer substrate comprises ceramic layers. Daniels shows wherein a

multi-layered impedance conversion substrate is in part of ceramic [column 2, lines 39-42]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have made the substrate of ceramic as suggested by Daniels in the substrate of the system of Ahn/Uchikoba/Utsumi/Cave, for the purpose of using a material which is commonly known to be well suited to handling high temperature cycling with minimal physical deformation due to thermal expansion.

Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,274,937) in view of Uchikoba (US 6,628,178) in further view of Utsumi et al. (US 6,091,310) in even further view of Cave et al. (US 7,190,083) in view of Juskey et al. (US 6,356,453).

Regarding claim 29, Ahn/Uchikoba/Utsumi/Cave disclose the method of claim 27. Ahn in view of Uchikoba in further view of Utsumi do not show wherein the at least one chip component and/or the at least one discrete circuit element is mechanically stabilized using a casting compound. Juskey et al. do disclose in Figure 5, wherein the at least one chip [522] component and/or the at least one discrete circuit element [536] is mechanically stabilized using a casting compound [536]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a casting compound as taught by Juskey in the system of Ahn/Uchikoba/Utsumi/Cave in order to provide a material which protects the electronic components from the ambient environment.

Response to Arguments

In regard to the remarks on page 11 of the arguments, it is asserted that Ahn does not show an impedance converter in Figure 1, but a, inductor capacitor network to nullify parasitic capacitances among other conversions show in the specification of Ahn. As it is known in the art, inductance, resistance, and capacitance are all instances of impedances, therefore any change in the input capacitance/inductance/resistance is by definition a change in impedance levels.

This argument for not showing newly amended claim limitations is also moot in view of the newly used art rejection.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDUARDO A. RODELA whose telephone number is (571)272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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